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PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Zanchi, et al.	Docket No:	TI-36597
Serial No:	10/680,883	Examiner:	TBD
Filed:	10/08/03	Art Unit:	TBD

For: THREE-TRANSISTOR NAND AND NOR GATES FOR TWO-PHASE CLOCK GENERATORS

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97 & 1.98

"EXPRESS MAIL" Mailing Label No.
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 and is addressed to: Assistant Commissioner for Patents, Washington, DC 20231 on 11-07-03

Sharlet Hurst

Sharlet Hurst

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

Applicants wish to bring to the attention of the Patent and Trademark Office the information noted on the enclosed PTO-1449. A copy of the noted references is enclosed herewith.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668, and please credit any excess fees to such Deposit Account. Any further necessary extension of time is hereby requested.

Respectfully submitted,

W. Daniel Swayze, Jr.
Attorney for Applicants
Reg. No. 34,478

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Dallas, TX 75265
(972) 917-5633

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete If Known	
Application Number	10/680,883
Filing Date	10/08/03
First Named Inventor	Zanchi
Group Art Unit	TBD
Examiner Name	TBD
Attorney Docket No.	TI-36597

U.S. PATENT DOCUMENTS

Exam. Initials*	Cite No.[1]	U.S. Patent Document Number	U.S. Patent Document Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA	6,542,017		Manganaro	04-01-2003	
	AB					
	AC					
	AD					
	AE					
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FOREIGN PATENT DOCUMENTS

Exam. Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Foreign Patent Document Number[4]	Foreign Patent Document Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
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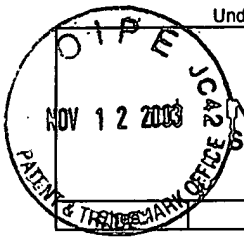

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Application Number	
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Exam. Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	CA	WESTE, et al, Principles of CMOS VLSI design, Addison-Wesley, Reading, MA, 1993.	
	CB	ZANCHI, et al, "Measurement and Spice prediction of sub-picosecond clock jitter in A-to-D converters, in Proceedings of the ISCAS 2003, Bangkok, Thailand, May 2003.	
	CC	SHINAGAWA, et al, Jitter analysis of high-speed sampling systems, IEEE Journal of Solid-State Circuits, vol. 25, no. 1, Feb 1990, pp. 220-224.	
	CD	MCNEILL, Jitter in ring oscillators, IEEE Journal of Solid-State Circuits, vol. 32, no. 6, June 1997, pp. 870-879.	
	CE	SEDRA, et al, Microelectroinc circuits, Sounders College Publishing, Orlando, FL, 1991.	
	CF	JOHNSON, A symmetric CMOS NOR gate for high-speed applications, IEEE Journal of Solid-State Circuits, vol. 23, no. 5, Oct 1988, pp. 1233-1236.	
	CG	MANGANARO, An improved phase clock generator for interleaved and double-sampled switched-capacitor circuits, in Proceedings of the ICECS 2001, Malta, Sep. 2001, pp. 1553-1556.	
	CH		
	CI		
	CJ		

Examiner Signature		Date Considered	

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